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10/658,595	09/09/2003	Paul Elliott	851963.413	1920

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SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 5400
SEATTLE, WA 98104

EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,595	ELLIOTT, PAUL	
	Examiner	Art Unit	
	NIMESH G. PATEL	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4-7, 13-14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connell et al.(US 6,208,703), in view of Fritz et al.(US 2002/0016850).

3. Regarding claim 1, O'Connell discloses a bridge circuit for use in retiming in a semiconductor integrated circuit, the bridge circuit comprising: an initiator interface(Figure 1, Top Interface); a target interface(Figure 1, Bottom Interface); a storage buffer circuit(Figure 1, 10) having a data input connected to the initiator interface and a data output connected to the target interface, and having a plurality of storage locations; and a storage buffer control circuit associated with the storage buffer circuit; the storage buffer control circuit comprising: a write pointer register(Figure 1, 40) connected to the storage buffer circuit and clocked at the storage buffer input clock rate(Figure 1, Application clock) to control the storage location at which data is written into the storage buffer circuit; a read pointer register(Figure 1, 42) connected to the storage buffer circuit and clocked at the storage buffer output clock rate(Figure 1, PCI clock) to control the storage location from which data is read from the storage buffer circuit; a first retiming circuit(Figure 1, 44) coupled to the output of the read pointer register to retime the output of the read pointer register with reference to the storage buffer input clock rate(Figure 1, Application clock); a second retiming circuit(Figure 1, 50) coupled to the output of the write pointer register to retime the output of the write pointer register with reference to the storage buffer output clock rate(Figure 1, PCI clock); a first comparator(Figure 1, 48, 46, 56) connected

to receive and compare the outputs of the write pointer register and the first retiming circuit and to provide an output(Figure 1, 49) dependent thereon; a second comparator(Figure 1, 52) connected to receive and compare the outputs of the read pointer register and the second retiming circuit and to provide an output(Figure 1, 54) dependent thereon; write control logic connected to receive the output of the first comparator and connected to the write pointer register to increment the count held in the write pointer register in dependence upon the output of the first comparator(Column 3, Line 53, Column 4, Lines 17-23); and read control logic connected to receive the output of the second comparator and connected to the read pointer register to increment the count held in the read pointer register in dependence upon the output of the second comparator(Column 5, Lines 54-67; Column 6, Lines 6-8); and wherein the write control logic in the storage buffer control circuit is adapted to control the write pointer register such that data, making up a data packet, received at the data input of the associated storage buffer circuit is written into successive storage locations of the storage buffer circuit as the data is received so long as the storage locations are not all full(Column 4, Lines 31-36), and the read control logic in the storage buffer control circuit is adapted to control the read pointer register such that data in the storage locations are read from successively and the contents applied to the data output of the storage buffer circuit(Column 6, Lines 7-10).

O'Connell does not specifically disclose that the storage locations are read only after a predetermined time delay, the time delay being such that a complete stat packet without gaps is applied to the data output. However, Fritz discloses storage locations being read after a predetermined time delay(Paragraph 13). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of O'Connell and Fritz to wait to read the storage locations after a predetermined delay since this is typically done in FIFOs to prevent

under run and to increase tolerance for delays that may be occasioned by latency and overhead.

4. Regarding claim 2, Fritz discloses a bridge circuit wherein the predetermined time delay is a predetermined number of clock cycles of either buffer input or output clock(Paragraph 13).

5. Regarding claim 4, Fritz discloses a bridge circuit, in which the read control logic also causes all the full storage locations to be read from on receipt of an end-of-packet signal(Paragraph 45).

6. Regarding claim 5, O'Connell discloses a bridge circuit, in which the comparators provide outputs indicating at least when the storage buffer circuit is full and is empty(Column 6, Lines 11-16).

7. Regarding claim 6, O'Connell discloses a bridge circuit, in which the maximum number of storage locations to be made available simultaneously is predetermined, the write control logic is adapted to determine when the storage buffer circuit is full(Column 4, Lines 31-36).

8. Regarding claim 7, O'Connell discloses a bridge circuit, in which each retiming circuit includes a Gray coder clocked at the input clock rate of the retiming circuit.(Column 5, Lines 43-44).

9. Regarding claim 13, Fritz discloses a bridge circuit, further comprising a second storage buffer circuit having a data input connected to the target interface and a data output connected to the initiator interface and a data output connected to the initiator interface and having a plurality of storage locations, and a second storage buffer control circuit similar to the first-mentioned storage buffer control circuit connected to control the second storage buffer circuit(Figure 3).

10. Regarding claim 14, O'Connell discloses a semiconductor integrated circuit comprising at least one bridge circuit in accordance with claim 1(Figure 1).

11. Regarding claim 21, O'Connell discloses a bridge circuit for use in retiming in a semiconductor integrated circuit, the bridge circuit comprising: an initiator interface(Figure 1, Top Interface); a target interface(Figure 1, Bottom Interface); a storage buffer circuit(Figure 1, 10) having a data input connected to the initiator interface and a data output connected to the target interface, and having a plurality of storage locations; and a storage buffer control circuit associated with the storage buffer circuit; the storage buffer control circuit comprising: a write pointer register(Figure 1, 40) coupled to the storage buffer circuit and clocked at the storage buffer input clock rate(Figure 1, Application clock), the write pointer register configurable to hold a first identifier(address) of a storage location at which data is written into the storage buffer circuit; a read pointer register(Figure 1, 42) coupled to the storage buffer circuit and clocked at the storage buffer output clock rate(Figure 1, PCI clock), the read pointer register configurable to hold a second identifier(address) of a storage location at which data is written into the storage buffer circuit; a first retiming circuit(Figure 1, 44) coupled to the output of the read pointer register to retime the output of the read pointer register with reference to the storage buffer input clock rate(Figure 1, Application clock); a second retiming circuit(Figure 1, 50) coupled to the output of the write pointer register to retime the output of the write pointer register with reference to the storage buffer output clock rate(Figure 1, PCI clock); a first comparator(Figure 1, 48, 46, 56) connected to receive and compare the outputs of the write pointer register and the first retiming circuit and to provide an output(Figure 1, 49) dependent thereon; a second comparator(Figure 1, 52) connected to receive and compare the outputs of the read pointer register and the second retiming circuit and to provide an output(Figure 1, 54) dependent thereon; write control logic connected to receive the output of the first comparator and connected to the write pointer register to increment the count held in the write pointer register in dependence upon the output of the first comparator(Column 3, Line 53, Column 4, Lines 17-23);

and read control logic connected to receive the output of the second comparator and connected to the read pointer register to increment the count held in the read pointer register in dependence upon the output of the second comparator(Column 5, Lines 54-67; Column 6, Lines 6-8); and wherein the write control logic in the storage buffer control circuit is adapted to control the write pointer register such that data, making up a data packet, received at the data input of the associated storage buffer circuit is written into successive storage locations of the storage buffer circuit as the data is received so long as the storage locations are not all full(Column 4, Lines 31-36), and the read control logic in the storage buffer control circuit is adapted to control the read pointer register such that data in the storage locations are read from successively and the contents applied to the data output of the storage buffer circuit(Column 6, Lines 7-10).

O'Connell does not specifically disclose that the storage locations are read only after a predetermined time delay, the time delay being such that a complete stat packet without gaps is applied to the data output. However, Fritz discloses storage locations being read after a predetermined time delay(Paragraph 13). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of O'Connell and Fritz to wait to read the storage locations after a predetermined delay since this is typically done in FIFOs to prevent under run and to increase tolerance for delays that may be occasioned by latency and overhead.

12. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connell, in view of Fritz, and in further view of Sadowski.

13. Regarding claim 8, O'Connell does not specifically disclose a bridge circuit, in which each retiming circuit is adapted to provide a plurality of possible degrees of retiming, and including a mode signal input for receiving a mode signal indicating the currently required degree of retiming, the retiming circuit being responsive to the mode signal to provide the

required degree of retiming. However O'Connell discloses a variety of methods can be used to implement the synchronization blocks (Column 5, Lines 42-43) and Sadowski discloses a plurality of possible degrees of retiming, and including a mode signal input for receiving a mode signal indicating the currently required degree of retiming, the retiming circuit being responsive to the mode signal to provide the required degree of retiming(Figure 1; Figure 5, 506, 508). It would have been obvious to one of ordinary skill in the art to use plurality of possible degrees of timing, since this would allow various clock domains to be synchronized depending on the clock differences.

14. Regarding claim 9, Sadowski discloses a bridge circuit, in which each retiming circuit includes two retiming elements connected in cascade, and a selector, the selector being connected to receive the input to the retiming elements and the output of each of the retiming elements and to select one of its inputs as the output in dependence upon the mode signal (Figure 1).

15. Regarding claim 10, Sadowski discloses a bridge circuit, in which the mode signal is adapted to be changed during operation of the bridge circuit (Paragraph 18).

16. Regarding claim 11, Sadowski discloses a bridge circuit, further comprising a strobe retiming circuit connected to receive a strobe signal and retime it relative to the initiator clock, an edge detector for detecting an edge in the strobe signal, a mode signal timing circuit for timing the mode signal relative to the output of the edge detector, and a mode signal change detection circuit connected to the output of the mode signal timing circuit to detect a change in the mode signal and to provide a change signal in response thereto (Paragraph 18).

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connell, in view of Fritz, and in further view of Cavanna et al.(US 6,208,703).

18. Regarding claim 12, O'Connell and Fritz do not specifically disclose a bridge circuit, further comprising a bypass for the storage buffer circuit, and a selector for selecting either the storage buffer circuit or the bypass in accordance with a mode signal received at an input(Figure 1). However, Cavanna discloses a bypass for the storage buffer circuit, and a selector for selecting either the storage buffer circuit or the bypass in accordance with a mode signal received at an input(Column 8, Lines 27-46). It would have been obvious to one of ordinary skill in the art to include a bypass circuit, as disclosed by Cavanna, in the system of O'Connell and Fritz, since this would enable the system to bypass synchronization in the case where the clock domains to the interface is the same.

19. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connell, in view of Fritz, and in further view of Sadowski.

20. Regarding claim 15, O'Connell discloses a bridge circuit for use in retiming in a semiconductor integrated circuit, the bridge circuit comprising: an initiator interface(Figure 1, Top Interface); a target interface(Figure 1, Bottom Interface); a storage buffer circuit(Figure 1, 10) having a data input connected to the initiator interface and a data output connected to the target interface, and having a plurality of storage locations; and a storage buffer control circuit associated with the storage buffer circuit; the storage buffer control circuit comprising: a write pointer register(Figure 1, 40) connected to the storage buffer circuit and clocked at the storage buffer input clock rate(Figure 1, Application clock) to control the storage location at which data is written into the storage buffer circuit; a read pointer register(Figure 1, 42) connected to the storage buffer circuit and clocked at the storage buffer output clock rate(Figure 1, PCI clock) to control the storage location from which data is read from the storage buffer circuit; a first retiming circuit(Figure 1, 44) coupled to the output of the read pointer register to retime the output of the read pointer register with reference to the storage buffer input clock rate

comprising one or more retiming buffers(Figure 1, Application clock); a second retiming circuit(Figure 1, 50) coupled to the output of the write pointer register to retime the output of the write pointer register with reference to the storage buffer output clock rate(Figure 1, PCI clock); a first comparator(Figure 1, 48, 46, 56) connected to receive and compare the outputs of the write pointer register and the first retiming circuit and to provide an output(Figure 1, 49) dependent thereon; a second comparator(Figure 1, 52) connected to receive and compare the outputs of the read pointer register and the second retiming circuit and to provide an output(Figure 1, 54) dependent thereon; write control logic connected to receive the output of the first comparator and connected to the write pointer register to increment the count held in the write pointer register in dependence upon the output of the first comparator(Column 3, Line53, Column 4, Lines 17-23); and read control logic connected to receive the output of the second comparator and connected to the read pointer register to increment the count held in the read pointer register in dependence upon the output of the second comparator(Column 5, Lines 54-67; Column 6, Lines 6-8).

O'Connell does not specifically disclose that the storage locations is only read after a predetermined time delay, the time delay being such that a complete stat packet without gaps is applied to the data output. However, Fritz discloses storage locations being read after a predetermined time delay(Paragraph 13). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of O'Connell and Fritz to wait to read the storage locations after a predetermined delay since this is typically done in FIFOs to prevent under run and to increase tolerance for delays that may be occasioned by latency and overhead.

O'Connell and Fritz do not specifically disclose a selector connected to receive inputs from each of the retiming and storage buffer control circuit that is adapted to control the

selectors such that zero or more retiming buffers are selectively in the path from the read or write pointer registers to the comparators. However, O'Connell discloses a variety of methods can be used to implement the synchronization blocks(Column 5, Lines 42-43) and Sadowski discloses a selector connected to receive inputs from each of the retiming and storage buffer control circuit that is adapted to control the selectors such that zero or more retiming buffers are selectively in the path from the read or write pointer registers to the comparator(Figure 1). It would have been obvious to one of ordinary skill in the art to use plurality of possible degrees of timing, since this would allow various clock domains to be synchronized depending on the clock differences.

21. Regarding claim 16, Sadowski discloses a bridge circuit, in which each retiming circuit is adapted to provide a plurality of possible degrees of retiming, and including a mode signal input for receiving a mode signal indicating the currently required degree of retiming, the retiming circuit being responsive to the mode signal to provide the required degree of retiming(Figure 1).

22. Regarding claim 17, Sadowski discloses a bridge circuit, in which each retiming circuit includes two retiming elements connected in cascade, and a selector, the selector being connected to receive the input to the retiming elements and the output of each of the retiming elements and to select one of its inputs as the output in dependence upon the mode signal(Figure 1).

23. Regarding claim 18, Sadowski discloses a bridge circuit, in which the mode signal is adapted to be changed during operation of the bridge circuit(Paragraph 18).

24. Regarding claim 19, O'Connell discloses a bridge circuit, wherein each retiming buffer comprises a D-type flip-flop for each bit in the pointer register output(Column 5, Lines 43-50), and Sadowski discloses zero or more D-type flip-flops are selectively chosen for retiming(Figure 1).

25. Regarding claim 20, Sadowski discloses a bridge circuit, wherein selectively 0, 1 or 2 D-type flip-flops are selected for retiming(Figure 1).

Response to Arguments

26. Applicant's arguments filed November 4, 2008 have been fully considered but they are not persuasive.

27. Applicant argues that O'Connell does not show incrementing the write pointer register based on the current position of the write pointer and a retiming signal from the read domain. However, this is not recited in the claims. The claim recites "write control logic connected to receive the output of the first comparator and connected to the write pointer register to increment the count held in the write pointer register in dependence upon the output of the first comparator." O'Connell does disclose write control logic connected to receive the output of the first comparator and connected to the write pointer register to increment the count held in the write pointer register in dependence upon the output of the first comparator(The write pointer register is incremented in dependence on the output of the comparator(Column 4, Lines 59-62; Column 5, Lines 16-20).

28. Applicant further discloses argues that O'Connell does not show incrementing the read pointer register. The claim recites "write control logic connected to receive the output of the second comparator and connected to the read pointer register to increment the count held in the read pointer register in dependence upon the output of the second comparator." O'Connell does disclose read control logic connected to receive the output of the second comparator and connected to the read pointer register to increment the count held in the read pointer register in dependence upon the output of the second comparator(The read pointer register is incremented in dependence on the output of the comparator(Column 5, Lines 54-67; Column 6, Lines 6-8).

29. Applicant has added new claim 21 and argues that O'Connell does not show the write pointer register holding a first identifier and read pointer register to hold second identifier, different from the first identifier. However, O'Connell does disclose the write pointer register holding a first identifier and read pointer register to hold second identifier, different from the first identifier(Column 5, Lines 24-40; The identifiers, i.e. addresses, stored in the register are different from one another).

Conclusion

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIMESH G. PATEL whose telephone number is (571)272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rinehart H. Mark can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nimesh G Patel/
Examiner, Art Unit 2111

/Glenn A. Auve/
Primary Examiner, Art Unit 2111